40-Gb/s Optical Receiver IC Chipset - including a Transimpedance Amplifier, a Differential Amplifier, and a Decision Circuit - using GaAs-based HBT Technology

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Abstract — **GaAs-based HBTs with an InGaP emitter were used to develop key components of a 40-Gb/s optical receiver: a transimpedance amplifier, a differential main amplifier, and a decision circuit. The frequency response of the transimpedance amplifier was flattened by inserting an RC series circuit at the input stage. As a result, the transimpedance amplifier module produced a well-opened 43-Gb/s eye diagram with 400 mVp-p dynamic range. The differential main amplifier and the decision circuit produced 43-Gb/s eye diagrams with a large dynamic range of 700 mVp-p, which is the first 40-Gb/s demonstration using GaAs-based HBTs. These three ICs are thus applicable to a 40-Gb/s optical receiver.**

I. Introduction

Data traffic carried on backbone optical networks has been increasing because of the rapid growth in the use of multimedia communications. A 40-Gb/s optical transmission system is under development to meet the future demand for long-haul DWDM transport systems. On the receiving side of such a system, the transimpedance amplifier, the main amplifier, and the decision circuit are the most speed-critical components, because these ICs need to handle the full transmission bandwidth for a data rate of 40 Gb/s. To achieve a system using packaged modules, each IC module must have, in addition to high-speed, broad-bandwidth performance, wide enough dynamic range to drive the succeeding components through connectors and cables. The GaAs-based HBT is a strong candidate for such IC modules, because of its excellent frequency characteristics, its large breakdown voltage of over 10 V, and its mature production technology with large-sized substrates.

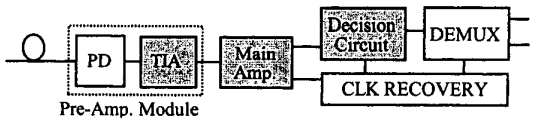

Fig. 1. 40-Gb/s optical transmission receiver

Accordingly, we have developed speed-critical ICs for 40-Gb/s optical receivers by using GaAs-based HBT technology. The fabricated ICs can operate at an over-40-Gb/s data rate with a large output voltage swing.

II. Device Characteristics

We previously developed high-speed GaAs-based HBTs [1] for over-40-Gb/s communication applications [2,3,4]. The heavily C-doped GaAs layer is selectively regrown in the extrinsic base contact region, thus drastically reducing base resistance. A 40-nm-thick graded InGaAs layer is used as the intrinsic base, so the base transist time is reduced. As a result, f_{max} is over 200 GHz and f_T is over 100 GHz at the same time. To increase the reliability, an AlGaAs emitter layer was replaced by an InGaP layer [5,6].

III. Circuit Design And Measurement Results

We developed a transimpedance amplifier, a main amplifier, and a decision circuit of the 40-Gb/s optical receiver system shown in Figure 1. These ICs are the key components that provide full transmission bandwidth for a data rate of 40 Gb/s. For accurate circuit design, we precisely extracted large-signal HBT model parameters incorporating the self-heating effect and Kirk effect. The extracted model parameters well exhibit HBT characteristics. Figure 2 shows DC I-V characteristics, and Figure 3 shows f_T versus I_C characteristics. As the figures show, there is good agreement between the measured and simulated characteristics.

A. Transimpedance Amplifier

Figure 4 shows the circuit diagram of the transimpedance amplifier (TIA), which consists of a transimpedance input stage, two emitter-followers, and a 50-Ω-impedance-matching output stage. We simulated the TIA including wire bonding inductance and a pin-

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photodiode (PD) circuit model with carrier transport effect. Transistor sizes and resistors were optimized to obtain larger output voltage swing and wider bandwidth. We flattened the frequency response by inserting an RC series circuit at the input stage of the TIA. We measured the S-parameters of the TIA with and without the RC circuit and transformed the transimpedance gain by taking into account the equivalent circuit of the pin-PD. Figure 5 shows the frequency response of transimpedance gain. The gain obtained in the TIA with the RC circuit is flatter, while that in the TIA without the RC circuit has an unwanted gain peaking, which causes ringing and time jitter in the output waveform.

Figure 6 shows a photograph of the fabricated TIA module including the pin-PD. The TIA chip area is 0.57X0.77 mm, its supply voltage is 5.3 V, and its power dissipation is 0.2 W. Figure 7 shows the 43-Gb/s output eye diagram of the TIA module. The eye diagram is well opened and the output swing is large, 400 mVp-p. This output voltage is large enough for driving the main amplifier.

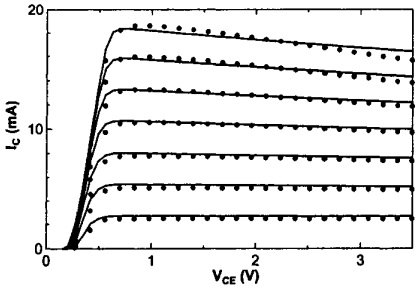

Fig. 2. Measured (dots) and simulated (lines) DC I-V characteristics of 1.6X9.6-μm emitter-area HBTs

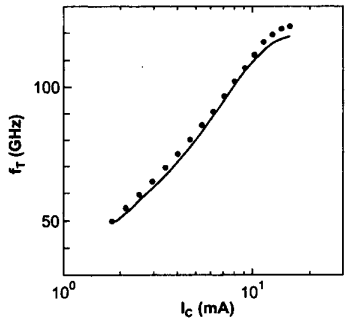

Fig. 3. Measured (dots) and simulated (lines) f_T versus I_C characteristics of 1.6X9.6-μm emitter-area HBTs

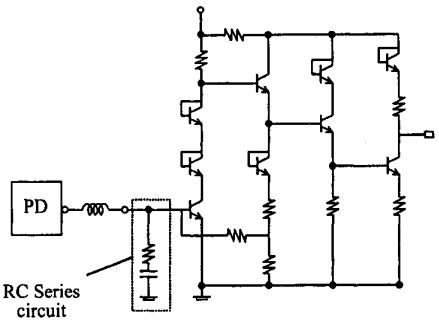

Fig. 4. Circuit diagram of a transimpedance amplifier

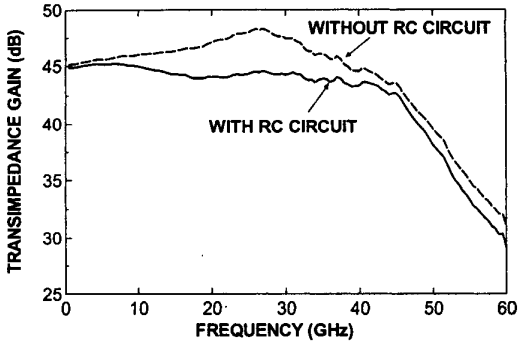

Fig. 5. Frequency response of a transimpedance amplifier

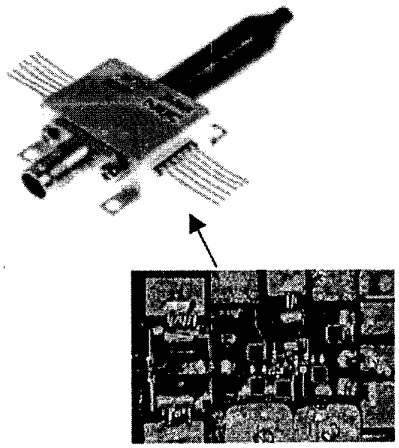

Fig. 6. Photograph of a transimpedance amplifier module

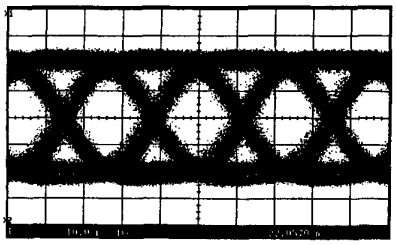

Figure. 7. 43-Gb/s output eye diagram of a transimpedance preamplifier module with a pin-photodiode

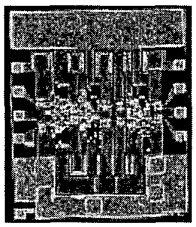

Figure. 8. Chip photograph of a differential main amplifier

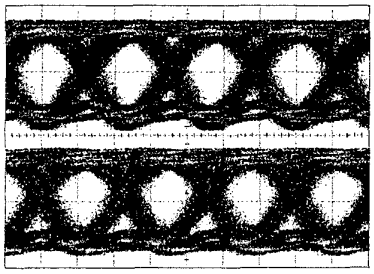

Figure. 9. 43-Gb/s output eye diagram of the differential main amplifier

B. Differential Main Amplifier

A differential amplifier is suitable for the main amplifier of the receiver because its dual output directly drives both the succeeding decision circuit and the clock recovery circuit at the same time. The fabricated main amplifier has three stages, each of which is composed of two emitter followers and a differential amplifier with a cascode configuration. The circuit layout was carefully thought out in order to flatten the frequency response.

Figure 8 shows a chip photograph of the differential main amplifier. The chip area is 1.2X1.4 mm, and the power dissipation is 1 W at –7-V supply voltage. Figure 9 shows the output eye diagram of the main amplifier for a 43-Gb/s output signal at an input voltage swing of 1 Vp-p measured by on-chip probes. The eye diagram is well opened with a large output swing of 700 mVp-p. To investigate the input sensitivity of the main amplifier, we evaluated the output eye diagram for various input-voltage swings. Eye diagrams with a 700-mVp-p output voltage swing were obtained for a wide-range input level from 0.17 Vp-p to 1 Vp-p. This wide input sensitivity and constant large output voltage mean that the differential amplifier is well suited as a limiting main amplifier.

C. Decision Circuit

Figure 10 shows a block diagram of the decision circuit, which consists of a two-stage input buffer, a master-slave D-type flip-flop, a two-stage output buffer, and a clock input stage. The differential amplifiers explained in the above section were used as the input and output buffers.

Figure 11 shows a photograph of the decision circuit. The chip area is 1.6X1.4 mm. Its typical supply voltage is -7 V, and its power dissipation is 2 W. Figure 12 shows the output eye diagram of the decision circuit for 43-Gb/s input signals measured by on-chip probes. The eye diagram is well opened with a large output swing of 700 mVp-p. We mounted the chip in a package and observed error-free operation at 43 Gb/s.

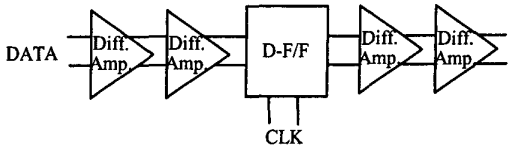

Figure. 10. Block diagram of a decision circuit

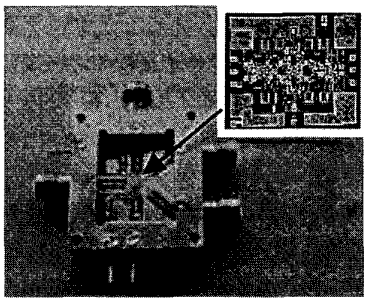

Figure. 11. Photograph of the decision circuit

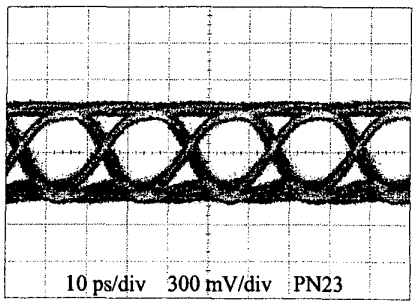

Figure. 12. 43-Gb/s output eye diagram of the decision circuit

IV. SUMMARY

We developed a transimpedance amplifier, a differential main amplifier, and a decision circuit for a 40-Gb/s optical receiver by using InGaP/InGaAs HBTs. The frequency response of the TIA was markedly flattened by inserting an RC series circuit at the input stage. As a result, the transimpedance amplifier module with a pin-photodiode produced a wide-open 43-Gb/s eye diagram with a large output voltage swing of 400 mVp-p. Under wide-range input amplitude from 0.17 Vp-p to 1 Vp-p, the differential main amplifier produced 40-Gb/s eye diagrams with 700 mVp-p output voltage swing. The decision circuit was designed by using the differential amplifier as the input and output buffer stage, resulting in a 43-Gb/s eye diagram with a voltage swing of 700 mVp-p. These ICs with high-speed performance and large dynamic range are suitable for the packaged modules of a 40-Gb/s optical receiver.

ACKNOWLEDGEMENT

The authors would like to thank K. Kuramoto and Y. Shiraishi for the device processing; S. Moribayashi, T. Kurioka, T. Isogai, M. Fujii, T. Maeda, T. Niwa, and H. Shimawaki for their useful discussions and technical support; and N. Baba and T. Chikuma for their support in measuring the transimpedance amplifier module. We also thank S. Fujita, A. Noda, H. Hirayama, M. Matsunoshita, S. Takemura, H. Ishiuchi, M. Mizuta, M. Fujiwara, I. Mito, M. Ogawa, T. Uji, T. Torikai, and M. Kuzuhara for their encouragement and support.

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